IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BOARD OF PATENT APPEALS AND INTERFERENCES

In re Application of: Welland et al.	
Application No.: 09/686,072	Examiner: LE, DINH THANH
Filed: October 11, 2000	Group Art Unit: 2816
	Attorney Docket No.: 75622.P0016

Title: METHOD AND APPARATUS FOR REDUCING INTERFERENCE

Mail Stop Appeal Brief-Patents
Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

APPEAL BRIEF

Applicant respectfully submits this Appeal Brief in triplicate, together with a Fee Transmittal and required fee. A Notice of Appeal and fee were previously filed.

Respectfully submitted,

By _____
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Date: 6-15-05

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I. Real Party in Interest

The real party in interest is the assignee, Silicon Laboratories Inc.

II. Related Appeals and Interferences

There are no related appeals or interferences.

III. Status of Claims

Claims 1, 3-4, 52-54, 66-79, and 81-85 are pending, and are under appeal.

Claims 2 and 80 have been canceled.

Claims 5-51 and 55-65 have been withdrawn in response to two restriction requirements.

IV. Status of Amendments

No amendments have been filed subsequent to the final rejection.

V. Summary of Claimed Subject Matter

While it is highly desirable to integrate various components on a single integrated circuit for cost, size, power dissipation, and performance considerations, barriers to integration exist. In some circuits, one significant problem relates to interference between components in the integrated circuit.

The present invention provides several techniques for reducing interference in integrated circuits. The Specification describes several techniques for reducing interference including:

- Using fixed-value, non-programmable counters rather than programmable counters, as well as clocking at least one of the counters at a slower rate. As described below in detail, this technique reduces digital current in one part of an integrated circuit that causes spurious tones in another part of the integrated circuit. (See FIG. 4, Spec., page 14, line 13 to page 15, line 23).

- Reducing the mutual inductance between current loops in digital circuitry and current loops in other circuitry. In one example, supply filters are used to reduce the area of these loops. (See FIGS. 5-6, Spec., page 15, line 25 to page 18, line 15).

- Reducing the mutual inductance between current loops in the digital circuitry and current loops in other circuitry. In one example, conduits are used to reduce the area of the transmit loops by containing high frequency current flowing through a signal line which spans a relatively large distance. (See FIGS. 8-15, Spec., page 18, line 17 to page 21, line 25).

- Using a cancellation technique to reduce interference. For this technique, components of a circuit are arranged such that magnetic fields of certain components cancel the

magnetic fields of other similar components. (See FIG. 16, Spec., page 22, lines 1-25).

- Managing the impedance of a circuit to reduce interference. In one example, replica circuitry is created and is controlled to always be in the opposite phase as the original circuitry. In this way, the impedance looking into the circuitry is approximately constant, independent of the state of the circuitry. (See FIGS. 17-18, Spec., page 22, line 17 to page 25, line 4).

- Containing leakage current in order to minimize the area of current loops. In one example, buffer circuits are used to confine leakage current within digital circuitry. (See FIGS. 19-23, Spec., page 25, line 6 to page 28, line 7).

- Using a filter at an integrated circuit clock input pin to reduce interference caused by a changing impedance at the clock input when the voltage of the clock input signal changes. (See FIG. 25, Spec., page 28, line 9 to page 29, line 14).

In two restriction requirements, the techniques listed above were restricted into seven groups. In the present patent application, the Applicants elected the first group listed above (using fixed-value, non-programmable counters rather than programmable counters), and the claims currently on appeal relate to this technique (although Applicants submit that independent claim 52 is generic).

The first technique listed above reduces digital current (e.g., current from digital circuitry on an integrated circuit) in one part of an integrated circuit that causes spurious tones in another part of the integrated circuit. One major source of digital current that causes interference are

divide-by-R counters, such as the divide-by-R counter 104 shown in FIG. 1. In typical prior art systems, divide-by-R counters are implemented using synchronous programmable counters. One problem with synchronous programmable counters is that the counter will have a large number of components. Another problem with synchronous programmable counters is that every flip-flop in the counter is clocked at the same speed. These problems result in interference. (Spec., page 14, lines 13-21).

The present invention reduces the digital current caused by divide-by-R counters by reducing the number of components in the divide-by-R counter. This is accomplished by using one or more fixed-value, non-programmable counters instead of programmable counters, and clocking at least one of the counters at a slower rate. (Spec., page 14, lines 21-24).

FIG. 1 is a block diagram illustrating a circuit having dividers 104 and 108. FIG. 4 is a similar block diagram, with the divide-by-R counter 104 replaced with two fixed-value, non-programmable counters 204 and 205. (Spec., page 15, lines 1-3). This arrangement results in less digital current, and thus less interference with other circuitry on an integrated circuit.

VI. Grounds of Rejection to be Reviewed on Appeal

A. Claims 1, 3-4, 52-54, 66-79, and 81-85 (including independent claims 1, 52, 66, 77, and 85) have been rejected under § 103(a) as being unpatentable over Bradley, US 6,087,865 (hereinafter "Bradley") in view of Dufour, US 6,111,470 (hereinafter "Dufour").

B. Claim 85 has been rejected under §112, second paragraph, as being indefinite. The examiner states that it is unclear how the divider can be "selected", how this step is read on the preferred embodiment, and that no such step is shown in the drawings.

VII. Argument

Claims 1, 3-4, 52-54, 66-79, and 81-85 are Patentable Over the Bradley and Dufour References Because the Cited References Fail to Teach or Suggest all of the Elements of the Claims

As mentioned above, claims 1, 3-4, 52-54, 66-79, and 81-85 have been rejected under § 103(a) as being unpatentable over Bradley in view of Dufour.

1. Brief Description of the Bradley and Dufour References

The Bradley reference relates to a programmable frequency divider (e.g., programmable frequency divider 199 in FIG. 5). The programmable frequency divider includes a frequency synthesizer 203 that provides an output signal having a desired frequency. The frequency synthesizer 203 uses a divide by Q frequency divider 221 and a divide by M frequency divider 222, where Q and M are integers that are selected by a user to achieve a desired output frequency. (Spec. Col. 6, line 42 to Col. 7, line23). The Dufour reference relates to phase-locked loop (PLL) circuits and systems for charge pump noise cancellation. (Col. 1, lines 5-7).

The examiner argues that it would have been obvious to implement the PLL circuit of Bradley on an integrated circuit as taught by Dufour, for the purpose of reducing size. The examiner also states that Bradley discloses a PLL circuit 203, comprising a first divider 221 and a second divider 220 (Figure 5 of Bradley).

To establish a prima facie case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to

combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the cited reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, not in applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991). See also, MPEP § 2143.

A motivation or suggestion to combine references is an "essential requirement" of a *prima facie* obviousness case. *C.R. Bard, Inc. v. M3 Sys., Inc.*, 48 U.S.P.Q.2d (BNA) 1225, 1232 (Fed. Cir. 1998). The PTO can satisfy its burden of showing obviousness "only by showing some objective teaching" leading to combination of references. *In re Fritch*, 23 U.S.P.Q.2d (BNA) 1780, 1783 (Fed. Cir. 1992). Furthermore, the showing of a motivation or suggestion to combine references "must be clear and particular." *In re Dembiczak*, 50 U.S.P.Q.2d (BNA) 1614, 1617 (Fed. Cir. 1999).

Applicants submit that the combination of Bradley and Dufour does not make the claims of the present invention unpatentable.

2. Independent Claim 1 is Patentable over Bradley in View of Dufour

Independent claim 1 recites a method of reducing interference in a circuit having a PLL, including "providing a divider circuit at the input of the PLL for dividing the frequency of an input signal by a desired amount" and "wherein the divider circuit is provided by placing first and second fixed-value dividers connected in series at the input of the PLL, wherein the first and second fixed-value dividers are configured to divide by respective first and second fixed non-programmable division factors." (Emphasis added).

In a previous amendment, applicants stated that the dividers 220 and 221 of Bradley are programmable dividers, not fixed-value or non-programmable dividers. In response, the examiner has taken the position that,

> "The argument is not persuasive because the dividers (221, 220) are not adjustable dividers so that the values (Q, R) are the fixed values after they are selected to accommodate with the frequency plan of a particular application." (Office Action, page 3, lines 16-18).

Using the examiner's definition of adjustable dividers, no divider would be "adjustable" unless the divisor continuously changed.

The Bradley patent (entitled "*Programmable Frequency Divider*") is very clear in describing dividers 221 and 220 as being programmable dividers. For example, when describing the divide by R divider 220 and the divide by Q divider 221 of Figure 5, Bradley states,

> "A user may select values for Q, R, and M so that equations 17 and 18 are satisfied for the user's desired value of N. The value for M may be altered depending on the selected value for FS. As with the circuit shown in FIG. 4, values of Q, R and M may be selected so that oscillators operating over the same frequency range may be used for the signal generator 200 as well as the VCO 210. (emphases added) (Bradley, Col. 7, lines 18-23).

Clearly, the division factors of the dividers 220 and 221 of Bradley are not fixed, and are designed to be changeable, as desired. Further, in the Office Action, the Examiner even points out that "the dividends (Q, R, M) of the dividers in the Bradley reference can be selectable." (Office Action, page 3, line 6, citing Bradley). Applicants' also point out that claim 1 recites "division factors", not "dividends." Bradley does not teach or suggest the use of fixed-value dividers or using fixed non-programmable division factors as claim 1 recites. For at least these reasons, it is submitted that independent claim 1 is allowable over the cited references. It is therefore also submitted that the claims depending from claim 1 are allowable.

3. Independent Claim 66 is Patentable over Bradley in View of Dufour

Independent claim 66 recites a method of reducing interference in a circuit formed on an integrated circuit that includes a divider circuit, including "providing a first fixed-value divider having an input and an output, wherein the first fixed-value divider is configured to divide by a first fixed non-programmable division factor," "providing a second fixed-value divider having an input and an output, wherein the second fixed-value divider is configured to divide by a second fixed non-programmable division factor," "generating a first output signal by applying an input frequency to the input of the first fixed-value divider to divide the input frequency by a first fixed value", and "generating a second output signal by applying the first output signal to the input of the second fixed-value divider to further divide the input frequency by a second fixed value." (Emphasis added).

For reasons similar to those argued above, Applicants submit that Independent claim 66 is patentable over Bradley in view of Dufour. Bradley discloses the dividers 221 and 220 as being programmable dividers (see the citation above). The divisors of the dividers 220 and 221 of Bradley are changeable or programmable, in contrast to the invention claimed in claim 66. For at least these reasons, it is submitted that independent claim 66 is allowable over the cited references. It is therefore also submitted that the claims depending from claim 66 are allowable.

4. Independent Claim 77 is Patentable over Bradley in View of Dufour

Independent claim 77 recites a circuit for reducing interference on an integrated circuit having a divider that includes "a first fixed-value non-programmable divider for receiving an

input signal and dividing the input signal by a first fixed amount," and "a second fixed-value non-programmable divider for receiving the divided signal from the first fixed-value divider and further dividing the input signal by a second fixed amount." (Emphasis added).

For reasons similar to those argued above, Applicants submit that Independent claim 77 is patentable over Bradley in view of Dufour. Bradley describes dividers 221 and 220 as being programmable dividers (see citation above). The divisors of the dividers 220 and 221 of Bradley are not fixed-value non-programmable dividers, as required by claim 77. For at least these reasons, it is submitted that independent claim 77 is allowable over the cited references. It is therefore also submitted that the claims depending from claim 77 are allowable.

5. Independent Claim 85 is Patentable over Bradley in View of Dufour

Independent claim 85 recites a method of reducing interference in a circuit formed on an integrated circuit including "selecting a divider in the circuit," "minimizing the number of circuit components used by the selected divider by using a plurality of fixed-value dividers rather than one or more programmable dividers, wherein each of the plurality of fixed-value dividers is configured to divide by a respective fixed non-programmable division factor," and "clocking at least one of the plurality of fixed-value dividers at a lower frequency than other fixed-value dividers in the circuit." (Emphasis added).

For reasons similar to those argued above, Applicants submit that Independent claim 85 is patentable over Bradley in view of Dufour. Bradley describes dividers 221 and 220 as being programmable dividers (see citation above). The divisors of the dividers 220 and 221 of Bradley are not fixed-value dividers, and are not each configured to divide by a fixed non-programmable

division factor, as claim 85 recites. For at least these reasons, it is submitted that independent claim 85 is allowable over the cited references.

6. Independent Claim 52 is Patentable over Bradley in View of Dufour

Claim 52 recites a method of integrating PLL circuitry for a wireless communication system onto a single integrated circuit including "forming the integrated circuit having PLL circuitry integrated on the integrated circuit, the PLL circuitry including VCO circuitry" and "applying one or more techniques to reduce interference present near the frequency of an output signal of the VCO circuitry." Neither Bradley nor Dufour teaches techniques for reducing interference present near the frequency of an output of VCO circuitry, as recited by claim 52. In addition, the Examiner has not made the allegation that Bradley and Dufour teach techniques for reducing interference present near the frequency of an output of VCO circuitry. Thus, neither reference is available for an obviousness rejection. *In re Royka*, 490 F.2d 981, 180 USPQ 580 (CCPA 1974). It is therefore submitted that claim 52 is also patentable over the Bradley and Dufour references. Since claims 53-54 depend from claim 52, it is also submitted that these claims are allowable.

Note also that dependent claim 53 recites "wherein the one or more techniques includes providing fixed divider circuitry for the PLL", and dependent claim 54 recites "wherein the divider circuitry further comprises first and second series connected fixed dividers." As argued above, Applicants submit that Bradley and Dufour do not teach or suggest using fixed divider circuitry.

Claim 85 is Clear and Definite Because the Specification and Drawings Make it Clear How a Divider can be Selected

As mentioned above, the examiner has rejected claim 85 under § 112 as being indefinite. The examiner states that it is unclear how the divider can be "selected", how this step is read on the preferred embodiment, and that no such step is shown in the drawings.

The Specification and Drawings make claim 85 is clear and definite. Claim 85 includes "selecting a divider in the circuit" and "minimizing the number of circuit components used by the selected divider by using a plurality of fixed-value dividers rather than one or more programmable dividers ..." FIG. 1 of the present application shows an example design of circuitry having a plurality of divide-by counters (counters 104 and 108, in this example). The Specification discusses various techniques for reducing the digital current that contributes to spurs, including reducing the interference caused by programmable counters. (Spec., page 14, lines 13-24). One technique for reducing interference caused by a programmable counter is to replace a programmable counter by one or more fixed-value counters, and clocking one of the timers at a slower rate. (Spec., page 14, lines 22-23). In one example described in the Specification, the counter 104 of the design illustrated in Figure 1 is selected and replaced by two fixed-value counters 204 and 205, resulting in the design shown in Figure 4. (FIGS. 1 and 4, Spec. page 15, lines 2-3). Therefore, claim 85 is clear, definite, as well as being supported by the drawings.

VIII. Claims Appendix

1. A method of reducing interference in a circuit having a PLL, wherein the circuit is formed on an integrated circuit, the method comprising the steps of:

providing a divider circuit at the input of the PLL for dividing the frequency of an input signal by a desired amount; and

wherein the divider circuit is provided by placing first and second fixed-value dividers connected in series at the input of the PLL, wherein the first and second fixed-value dividers are configured to divide by respective first and second fixed non-programmable division factors.

3. The method of claim 1, wherein the one of the dividers divides the input frequency by thirteen and the other divider divides the input frequency by five.

4. The method of claim 1, wherein:

the PLL is powered by a first voltage;

the divider circuit is powered by a second voltage; and

the second voltage is less than the first voltage.

52. A method of integrating PLL circuitry for a wireless communication system onto a single integrated circuit, comprising the steps of:

forming the integrated circuit having PLL circuitry integrated on the integrated circuit, the PLL circuitry including VCO circuitry; and

applying one or more techniques to reduce interference present near the frequency of an output signal of the VCO circuitry.

53. The method of claim 52, wherein the one or more techniques includes providing fixed divider circuitry for the PLL.

54. The method of claim 53, wherein the divider circuitry further comprises first and second series connected fixed dividers.

66. A method of reducing interference in a circuit formed on an integrated circuit that includes a divider circuit, the method comprising the steps of:

providing a first fixed-value divider having an input and an output, wherein the first fixed-value divider is configured to divide by a first fixed non-programmable division factor;

providing a second fixed-value divider having an input and an output, wherein the second fixed-value divider is configured to divide by a second fixed non-programmable division factor;

coupling the output of the first fixed-value divider to the input of the second fixed-value divider;

coupling the output of the second fixed-value divider to the circuit;

generating a first output signal by applying an input frequency to the input of the first fixed-value divider to divide the input frequency by a first fixed value; and

generating a second output signal by applying the first output signal to the input of the second fixed-value divider to further divide the input frequency by a second fixed value.

67. The method of claim 66, wherein the product of the first and second fixed values is sixty-five.

68. The method of claim 67, wherein the fixed values are five and thirteen.

69. The method of claim 66, wherein the first and second dividers are non-programmable dividers.

70. The method of claim 66, wherein the first divider is clocked at a first frequency, and the second divider is clocked at a frequency.

71. The method of claim 70, wherein the first frequency is greater than the second frequency.

72. The method of claim 71, wherein the second frequency is a function of the first fixed value.

73. The method of claim 66, wherein the first and second dividers are powered by a lower voltage than the remainder of the circuit.

74. The method of claim 66, wherein the circuit includes a PLL.

75. The method of claim 66, wherein the circuit is a frequency synthesizer.

76. The method of claim 66, wherein the circuit is a frequency synthesizer for a wireless communications device.

77. A circuit for reducing interference on an integrated circuit comprising:

circuitry formed on the integrated circuit having an input; and

a divider formed on the integrated circuit and coupled to the input of the circuitry, wherein the divider further comprises:

a first fixed-value non-programmable divider for receiving an input signal and dividing the input signal by a first fixed amount, and

a second fixed-value non-programmable divider for receiving the divided signal from the first fixed-value divider and further dividing the input signal by a second fixed amount.

78. The circuit of claim 77, wherein the product of the first and second amounts is sixty-five.

79. The circuit of claim 77, wherein the first amount is five and the second amount is thirteen.

81. The circuit of claim 77, wherein the first and second dividers are clocked at different frequencies.

82. The circuit of claim 81, wherein the second divider is clocked at a frequency that is a function of the first amount.

83. The circuit of claim 77, wherein the circuitry includes a PLL.

84. The circuit of claim 77, wherein the circuitry is a frequency synthesizer.

85. A method of reducing interference in a circuit formed on an integrated circuit, the circuit having one or more dividers, the method comprising the steps of:

selecting a divider in the circuit;

minimizing the number of circuit components used by the selected divider by using a plurality of fixed-value dividers rather than one or more programmable dividers, wherein each of the plurality of fixed-value dividers is configured to divide by a respective fixed non-programmable division factor; and

clocking at least one of the plurality of fixed-value dividers at a lower frequency than other fixed-value dividers in the circuit.

IX. Evidence Appendix

This section is not applicable.

X. Related Proceedings Appendix

This section is not applicable.

PTO/SB/17 (12-04v2)
Approved for use through 07/31/2006. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Effective on 12/08/2004.
Fees pursuant to the Consolidated Appropriations Act, 2005 (H.R. 4818).

FEE TRANSMITTAL
For FY 2005

☐ Applicant claims small entity status. See 37 CFR 1.27

TOTAL AMOUNT OF PAYMENT ($) 1,520.00

Complete if Known	
Application Number	09/686,072
Filing Date	10/11/2000
First Named Inventor	Welland, David R.
Examiner Name	LE, DINH THANH
Art Unit	2816
Attorney Docket No.	75622.P0016

METHOD OF PAYMENT (check all that apply)

☐ Check ☑ Credit Card ☐ Money Order ☐ None ☐ Other (please identify): _____

☐ Deposit Account Deposit Account Number: _____ Deposit Account Name: _____

For the above-identified deposit account, the Director is hereby authorized to: (check all that apply)

☐ Charge fee(s) indicated below ☐ Charge fee(s) indicated below, **except for the filing fee**

☐ Charge any additional fee(s) or underpayments of fee(s) under 37 CFR 1.16 and 1.17 ☐ Credit any overpayments

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FEE CALCULATION

1. BASIC FILING, SEARCH, AND EXAMINATION FEES

Application Type	FILING FEES Fee ($)	FILING FEES Small Entity Fee ($)	SEARCH FEES Fee ($)	SEARCH FEES Small Entity Fee ($)	EXAMINATION FEES Fee ($)	EXAMINATION FEES Small Entity Fee ($)	Fees Paid ($)
Utility	300	150	500	250	200	100	
Design	200	100	100	50	130	65	
Plant	200	100	300	150	160	80	
Reissue	300	150	500	250	600	300	
Provisional	200	100	0	0	0	0	

2. EXCESS CLAIM FEES

Fee Description	Fee ($)	Small Entity Fee ($)
Each claim over 20 (including Reissues)	50	25
Each independent claim over 3 (including Reissues)	200	100
Multiple dependent claims	360	180

Total Claims		Extra Claims	Fee ($)		Fee Paid ($)
_____	- 20 or HP =	_____	x _____	=	_____

HP = highest number of total claims paid for, if greater than 20.

Indep. Claims		Extra Claims	Fee ($)		Fee Paid ($)
_____	- 3 or HP =	_____	x _____	=	_____

HP = highest number of independent claims paid for, if greater than 3.

Multiple Dependent Claims Fee ($)	Multiple Dependent Claims Fee Paid ($)
_____	_____

3. APPLICATION SIZE FEE

If the specification and drawings exceed 100 sheets of paper (excluding electronically filed sequence or computer listings under 37 CFR 1.52(e)), the application size fee due is $250 ($125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).

Total Sheets		Extra Sheets		Number of each additional 50 or fraction thereof	Fee ($)		Fee Paid ($)
_____	- 100 =	_____	/ 50 =	_____ (round up to a whole number)	x _____	=	_____

4. OTHER FEE(S)

	Fees Paid ($)
Non-English Specification, $130 fee (no small entity discount)	
Other (e.g., late filing surcharge): Appeal Brief fee (500), extension of time fee (1020)	$1520.00

SUBMITTED BY

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